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The CMS electromagnetic calorimeter upgrade: high-rate readout with precise time and energy resolution

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Abstract

The electromagnetic calorimeter (ECAL) of the CMS detector has played an important role in the physics program of the experiment, delivering outstanding performance throughout data taking. The high-luminosity LHC will pose new challenges. The four to five-fold increase of the number of interactions per bunch crossing will require superior time resolution and noise rejection capabilities. For these reasons the electronics readout has been completely redesigned. A dual gain trans-impedance amplifier and an ASIC providing two 160 MHz ADC channels, gain selection, and data compression will be used in the new readout electronics. The trigger decision will be moved off-detector and will be performed by powerful and flexible FPGA processors, allowing for more sophisticated trigger algorithms to be applied. The upgraded ECAL will be capable of high-precision energy measurements throughout HL-LHC and will greatly improve the time resolution for photons and electrons above 10 GeV.

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The CMS electromagnetic calorimeter upgrade: high-rate readout with precise time and energy resolution

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ABSTRACT. The electromagnetic calorimeter (ECAL) of the CMS detector has played an important role in the physics program of the experiment, delivering outstanding performance throughout data taking. The high-luminosity LHC will pose new challenges. The four to five-fold increase of the number of interactions per bunch crossing will require superior time resolution and noise rejection capabilities. For these reasons the electronics readout has been completely redesigned. A dual gain trans-impedance amplifier and an ASIC providing two 160 MHz ADC channels, gain selection, and data compression will be used in the new readout electronics. The trigger decision will be moved off-detector and will be performed by powerful and flexible FPGA processors, allowing for more sophisticated trigger algorithms to be applied. The upgraded ECAL will be capable of high-precision energy measurements throughout HL-LHC and will greatly improve the time resolution for photons and electrons above 10 GeV.

KEYWORDS: Calorimeters; Front-end electronics for detector readout

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1 Introduction

The Compact Muon Solenoid (CMS) is an experiment located at CERN at the Large Hadron Collider (LHC). The central part of the CMS detector is a superconducting magnet which provides a magnetic field of 3.8T. Inside the solenoid are placed the tracker, closest to the beam pipe, followed by the electromagnetic calorimeter (ECAL) and the hadronic calorimeter (HCAL). Muon chambers are placed outside of the solenoid and are embedded in the steel return yoke. The sketch of the CMS detector is shown in figure 1. A detailed description of CMS detector can be found in ref. [1]. During the run 1 and run 2 periods of data taking, an integrated luminosity of 300 fb^{-1} was accumulated. Excellent performance was obtained for these data taking periods with constant monitoring and calibration. The energy resolution during run 2 (2016, 2017 and 2018) for electrons from Z-boson decays was at the level of 1.7% in the low pseudorapidity region. In order to compare the run 2 and run 1 resolution, the samples are reweighted to match the pileup distribution from 2017. The performance from run 2 is very close to the one from run 1 despite much larger pileup and ageing of the detector (figure 2).

In order to extend the reach of new physics searches and the precision Higgs boson coupling measurements, the LHC will be upgraded to increase its luminosity by a factor of five to seven to reach 10^{34} cm⁻² s⁻¹ [2]. The center-of-mass energy for proton-proton collisions will be also raised from 13 TeV to 14 TeV. The average number of interaction will be 250–300 and the radiation levels will be much higher than in the previous data taking periods. To meet the challenges of HL-LHC, all LHC experiments, including CMS, will be upgraded.

In section 2 the ECAL barrel readout architecture used so far will be described. In section 3, the upgraded electronics for HL-LHC will be presented, including descriptions of the new very front-end (VFE) and front-end (FE) cards and the upgraded off-detector electronics.



Figure 1. Schematic view of CMS detector.



Figure 2. Energy resolution with the refined calibration as a function of the pseudorapidity comparing the 2016, 2017, and 2018 run 2 data-taking periods (left) and run 2 with 2012 run 1 data-taking period in the barrel region (right).

2 The CMS ECAL readout

ECAL is a high granularity lead tungstate crystal calorimeter, designed to achieve excellent energy resolution for electrons and photons. It is composed of a central, barrel region, which consists of 61200 crystals and covers the pseudorapidity region $|\eta| < 1.48$, and two endcaps with 14648 crystals covering the range $1.48 < |\eta| < 3$.

The CMS ECAL barrel is divided into 36 supermodules and 2448 readout units (figure 3). The photodetectors used are avalanche photodiodes (APDs) in the barrel and vacuum phototriodes (VPTs) in the endcaps. A sketch of the current ECAL readout system is shown in figure 4.



Figure 3. Structure of the ECAL.



Figure 4. The CMS ECAL readout system.

In the barrel, two APDs are glued on one end of each crystal and connected through a Kapton cable to a VFE card. Each VFE card includes five readout channels consisting of a multi-gain preamplifiers (MGPA) and analog-to-digital converters (ADC). The MGPAs provide three different output gains (\times 1, \times 6, \times 12) for each APD, and the outputs are converted by a 12-bit, 40 MS/s ADC chip. The signals from five VFE cards are passed to a single FE card. On the FE card the trigger generator circuit based on an ASIC and an optical transceiver is placed. The output is sent to the DAQ and trigger system through the optical transceiver called FENIX.

3 The ECAL barrel readout chain upgrade for HL-LHC

In order to cope with the larger trigger decision latency (12.5 μ s instead of current 4 μ s) and larger L1 trigger rate (750 kHz compared to current 100 kHz) at HL-LHC, the ECAL barrel electronics

need to be modified. In addition, the new electronics have been designed to adapt to the new conditions and to maintain performance [3].

In the VFE card, the MGPA will be replaced by a Trans Impedance Amplifier (TIA) named CATIA which will improve discrimination between the electromagnetic signals and the ones coming from direct ionization in the APDs (spikes). The multi-channel ADC will be replaced by the LiTE-DTU ASIC (Lisbon-Torino ECAL Data Transmission Unit) that samples the signal at 160 MS/s with 12-bit resolution. For the upgraded FE card, the trigger primitive generation will be moved from on-detector electronics to the off-detector system. Moreover, for the data transmission the FE card will use Low Power Gigabit Transceiver (lpGBT) optical transceiver [4] and Versatile Link plus [5]. The upgraded off-detector electronics, based on the Barrel Calorimeter Processor (BCP) card [9], will use powerful FPGAs for detector read-out and to generate trigger primitives. The schematic view of the ECAL barrel electronics upgrade is shown in figure 5.



Figure 5. Schematic view of the new ECAL barrel electronics for HL-LHC.

3.1 CATIA ASIC

The CATIA (CAlorimeter TransImpedance Amplifier) is a fully analog ASIC designed in 130 nm CMOS technology. It features two output channels where one is for low energy signals (10 MeV–200 GeV) and the other is for high energy signals (10 MeV–2 TeV). The processing of signals from the APDs is done in three stages. The first stage converts the input current to a voltage using the high speed TIA. Following this step, the output is split into two channels with gains that differ by a factor of 10. The signals are routed to the LiTE DTU (described in the next section) by differential links.

The performance of the CATIA prototype has been tested in test beam campaigns at the H4/H2 beamline of the CERN SPS [6]. The test beam results have shown excellent performance of CATIA in terms of noise, linearity, and time resolution. The energy resolution matches with the resolution which has been obtained in beam tests with the legacy electronics [10], while a timing resolution of better than 30 ps is obtained for electrons with an energy greater than 50 GeV (figure 6) and complies with specifications.



Figure 6. Energy resolution (left) and time resolution (right) obtained in the test beam campaign with the CATIA ASIC connected to a commercial ADC.

3.2 LITE-DTU ASIC

The LiTE-DTU converts the analog output of CATIA to digital (ADC), selects one of the two gains for each time sample, compresses the data and transmits them to the FE card. This ASIC is built in 65 nm CMOS technology [7]. In order to convert, in parallel, the two outputs of the CATIA, the LiTE-DTU have two ADC IP blocks. The ADC, design by an external company, has 12-bit of resolution and a sampling frequency of 160 MHz. LiTE-DTU also includes a phase locked loop (PLL) for clock generation based on a design developed for the lpGBT chip. After conversion of the signal, the data transmission unit (DTU) selects between the two streams with different gains by looking for the highest non-saturated gain channel. In order to reduce the required bandwidth for the data transmission, the data are then compressed. Using a loss-less data compression mechanism, the reduction of the bandwidth is from 2.08 Gb/s to 1.08 Gb/s. Data packets from the LiTE-DTU are serialized to the FE board through differential electrical links at 1.28 Gb/s. LiTE-DTU is designed to sustain a total irradiation dose up to 20 kGy and it implements single-event upset (SEU) protection. The first prototype of the LiTE-DTU ASIC is tested was the late 2019.

3.3 Front-end board and back-end electronics upgrade

The FE card is designed for streaming the digitized data generated on the VFE to the back-end electronics system. The FE card contains four lpGBT ASICs. The new FE card will manage system initialization and control signals of the VFEs. In addition, it will provide the clock for the VFEs. The upgraded FE will no longer compute the trigger primitives as the data will now be streamed to the off-detector electronics at the full collision rate [8].

The off-detector system will be upgraded in order to handle the change in architecture and to deal with the higher transfer rates. On the BCP, implemented as an Advanced Telecommunications Computing Architecture (ATCA) blade, the FPGAs will be used to form the L1 trigger decision and

read out the detector. The BCP will be common between ECAL and the CMS hadronic calorimeter. It will provide the clock distribution and control to the FE card. BCP will also interface with the CMS data acquisition.

4 Conclusion

During LHC run 2, the CMS ECAL detector showed good performance despite increased pileup and radiation. Good energy resolution and good stability over time were maintained with constant calibration and monitoring. Nevertheless, for the pileup and radiation conditions that will be reached at HL-LHC, the replacement of the ECAL endcap with a new technology and an upgrade of the readout electronics of the barrel are needed. Replacing the readout electronics will ensure that ECAL complies with the new trigger requirements, has improved L1 capabilities, withstands the increased radiation, and mitigates pileup effects and APD noise. In addition, the upgrade will allow ECAL to maintain excellent energy resolution and have improved timing resolution. For the upgrade of the VFE two custom ASICs, CATIA and LiTE-DTU, have been designed. New FE and off-detector electronics have been developed. Prototypes have been tested and further tests are under way.

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